Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Previously Presented) A ferroelectric, non-volatile, SR flip-flop as in claim 81 in which the first logic gate comprises a first NAND gate and the second logic gate comprises a second NAND gate.

2. (Currently Amended) The SR flip-flop of claim 1 in which the first NAND gate comprises:

a first P-channel transistor having a gate coupled to the first input, a source coupled to a voltage source, and a drain coupled to the output;

a second P-channel transistor having a gate coupled to the second input, a source coupled to the voltage source, and a drain coupled to the output;

a first N-channel transistor having a drain coupled to the output, a gate coupled to the second input, and a source ~~coupled to the internal circuit node~~; and

a second N-channel transistor having a drain coupled to the source of the first N-channel transistor ~~internal circuit node~~, a gate coupled to the first input, and a source coupled to ground.

3. (Currently Amended) The SR flip-flop of claim 1 in which the first NAND gate comprises:

a first P-channel transistor having a gate coupled to the first input, a source coupled to a first controlled power supply, and a drain coupled to the output;

a second P-channel transistor having a gate coupled to the second input, a source coupled to the first controlled power supply, and a drain coupled to the output;

a first N-channel transistor having a drain coupled to the output, a gate coupled to the second input, and a source ~~coupled to the internal circuit node~~; and

a second N-channel transistor having a drain coupled to the source of the first N-channel transistor ~~internal circuit node~~, a gate coupled to the first input, and a source coupled to a second controlled power supply.

4. (Currently Amended) The SR flip-flop of claim 1 in which the second NAND gate comprises:

a first P-channel transistor having a gate coupled to the first input, a source coupled to a voltage source, and a drain coupled to the output;

a second P-channel transistor having a gate coupled to the second input, a source coupled to the voltage source, and a drain coupled to the output;

a first N-channel transistor having a drain coupled to the output, a gate coupled to the second input, and a source ~~coupled to the internal circuit node~~; and

a second N-channel transistor having a drain coupled to the source of the first N-channel transistor ~~internal circuit node~~, a gate coupled to the first input, and a source coupled to ground.

5. (Currently Amended) The SR flip-flop of claim 1 in which the second NAND gate comprises:

a first P-channel transistor having a gate coupled to the first input, a source coupled to a first controlled power supply, and a drain coupled to the output;

a second P-channel transistor having a gate coupled to the second input, a source coupled to the first controlled power supply, and a drain coupled to the output;

a first N-channel transistor having a drain coupled to the output, a gate coupled to the second input, and a source ~~coupled to the internal circuit node~~; and

a second N-channel transistor having a drain coupled to the source of the first N-channel transistor ~~internal circuit node~~, a gate coupled to the first input, and a source coupled to a second controlled power supply.

6. (Original) The SR flip-flop of claim 1 in which the ferroelectric capacitor circuit comprises:

a first ferroelectric capacitor coupled between the internal circuit node of the first NAND gate and ground;

a second ferroelectric capacitor coupled between the internal circuit node of the second NAND gate and ground; and

a third ferroelectric capacitor coupled between the internal circuit nodes of the first and second NAND gates.

7. (Original) The SR flip-flop of claim 1 in which the ferroelectric capacitor circuit comprises:

a first ferroelectric capacitor coupled between the internal circuit node of the first NAND gate and ground;

a second ferroelectric capacitor coupled between the internal circuit node of the second NAND gate and ground; and

third and fourth serially-coupled matched ferroelectric capacitors coupled between the internal circuit nodes of the first and second NAND gates.

8. (Currently Amended) The SR flip-flop of claim 1 further comprising means for selectively coupling the ferroelectric capacitor circuit ~~to the internal nodes of the first and second NAND gates~~.

9. (Currently Amended) The SR flip-flop of claim 1 further comprising a pass gate circuit for selectively coupling the ferroelectric capacitor circuit ~~to the internal nodes of the first and second NAND gates~~.

10. (Original) The SR flip-flop of claim 1 further comprising a precharge circuit coupled to the first and second NAND gates.

11. (Original) The SR flip-flop of claim 1 further comprising an equalization circuit coupled to the first and second NAND gates.

12. (Original) The SR flip-flop of claim 1 further comprising a gate control circuit coupled to the first and second NAND gates.

13. (Original) The SR flip-flop of claim 1 in which the first and second NAND gates further comprise an internal drive isolation circuit.

14. (Previously Presented) A ferroelectric, non-volatile, SR flip-flop as in claim 81 in which the first logic gate comprises a first NOR gate and the second logic gate comprises a second NOR gate.

15. (Currently Amended) The SR flip-flop of claim 14 in which the first NOR gate comprises:

a first P-channel transistor having a gate coupled to the first input, a source coupled to a voltage source, and a drain ~~coupled to the internal node~~;

a second P-channel transistor having a gate coupled to the second input, a source coupled to the drain of the first P-channel transistor ~~internal node~~, and a drain coupled to the output;

a first N-channel transistor having a drain coupled to the output, a gate coupled to the first input, and a source coupled to ground; and

a second N-channel transistor having a drain coupled to the output, a gate coupled to the second input, and a source coupled to ground.

16. (Currently Amended) The SR flip-flop of claim 14 in which the first NOR gate comprises:

a first P-channel transistor having a gate coupled to the first input, a source coupled to a first controlled power supply, and a drain ~~coupled to the internal circuit node~~;

a second P-channel transistor having a gate coupled to the second input, a source coupled to the drain of the first P-channel transistor ~~internal circuit node~~, and a drain coupled to the output;

a first N-channel transistor having a drain coupled to the output, a gate coupled to the first input, and a source coupled to a second controlled power supply; and

a second N-channel transistor having a drain coupled to the output, a gate coupled to the second input, and a source coupled to the second controlled power supply.

17. (Currently Amended) The SR flip-flop of claim 14 in which the second NOR gate comprises:

a first P-channel transistor having a gate coupled to the first input, a source coupled to a voltage source, and a drain ~~coupled to the internal circuit node~~;

a second P-channel transistor having a gate coupled to the second input, a source coupled to the drain of the first P-channel transistor ~~internal circuit node~~, and a drain coupled to the output;

a first N-channel transistor having a drain coupled to the output, a gate coupled to the first input, and a source coupled to ground; and

a second N-channel transistor having a drain coupled to the output, a gate coupled to the second input, and a source coupled to ground.

18. (Currently Amended) The SR flip-flop of claim 14 in which the second NOR gate comprises:

a first P-channel transistor having a gate coupled to the first input, a source coupled to a first controlled power supply, and a drain ~~coupled to the internal circuit node~~;

a second P-channel transistor having a gate coupled to the second input, a source coupled to the drain of the first P-channel transistor ~~internal circuit node~~, and a drain coupled to the output;

a first N-channel transistor having a drain coupled to the output, a gate coupled to the first input, and a source coupled to a second controlled power supply; and

a second N-channel transistor having a drain coupled to the output, a gate coupled to the second input, and a source coupled to the second controlled power supply.

19. (Previously Presented) The SR flip-flop of claim 14 in which the ferroelectric capacitor circuit comprises:

a first ferroelectric capacitor coupled between the second input of the first NOR gate and ground;

a second ferroelectric capacitor coupled between the second input of the second NOR gate and ground; and

a third ferroelectric capacitor coupled between the second inputs of the first and second NOR gates.

20. (Previously Presented) The SR flip-flop of claim 14 in which the ferroelectric capacitor circuit comprises:

a first ferroelectric capacitor coupled between the second input of the first NOR gate and ground;

a second ferroelectric capacitor coupled between the second input of the second NOR gate and ground; and

third and fourth serially-coupled matched ferroelectric capacitors coupled between the second inputs of the first and second NOR gates.

21. (Currently Amended) The SR flip-flop of claim 14 further comprising means for selectively coupling the ferroelectric capacitor circuit ~~to the second inputs of the first and second NOR gates~~.

22. (Currently Amended) The SR flip-flop of claim 14 further comprising a pass gate circuit for selectively coupling the ferroelectric capacitor circuit ~~to the second inputs of the first and second NOR gates~~.

23. (Previously Presented) The SR flip-flop of claim 14 further comprising a precharge circuit coupled to the first and second NOR gates.

24. (Previously Presented) The SR flip-flop of claim 14 further comprising an equalization circuit coupled to the first and second NOR gates.

25. (Previously Presented) The SR flip-flop of claim 14 further comprising a gate control circuit coupled to the first and second NOR gates.

26. (Previously Presented) The SR flip-flop of claim 14 in which the first and second NOR gates further comprise an internal drive isolation circuit.

27. (Previously Presented) The SR flip-flop of claim 81 further comprising:

a J input;

a K input;

a first NAND gate having a first input coupled to the Q output of the SR flip-flop, a second input coupled to the K input, a third input for receiving a clock signal and an output coupled to the set input of the SR flip-flop; and

a second NAND gate having a first input for receiving the clock signal, a second input coupled to the J input, a third input coupled to the complementary Q output of the SR flip-flop and an output coupled to the reset input of the SR flip-flop.

28. (Previously Presented) The SR flip-flop of claim 27 in which the SR flip-flop comprises a NAND-gate based flip-flop.

29. (Previously Presented) The SR flip-flop of claim 27 in which the SR flip-flop comprising a NOR-gate based flip-flop.

30. (Previously Presented) The SR flip-flop of claim 27 further comprising a first controlled power supply coupled to the SR flip-flop.

31. (Previously Presented) The SR flip-flop of claim 30 further comprising a second controlled power supply coupled to the SR flip-flop.

32. (Previously Presented) The SR flip-flop of claim 27 in which the ferroelectric capacitor circuit comprises first, second, and third ferroelectric capacitors.

33. (Previously Presented) The SR flip-flop of claim 32 in which one of the ferroelectric capacitors comprises two serially-coupled matched ferroelectric capacitors.

34. (Previously Presented) The SR flip-flop of claim 32 further comprising means for selectively coupling the ferroelectric capacitor circuit.

35. (Previously Presented) The SR flip-flop of claim 27 further comprising a precharge circuit coupled to the SR flip-flop.

36. (Previously Presented) The SR flip-flop of claim 27 further comprising an equalization circuit coupled to the SR flip-flop.

37. (Previously Presented) The SR flip-flop of claim 27 further comprising a gate control circuit coupled to the SR flip-flop.

38. (Previously Presented) The SR flip-flop of claim 27 in which the SR flip-flop further comprises an internal drive isolation circuit.

39. (Previously Presented) The SR flip-flop of claim 27 further comprising:

a slave JK flip-flop interposed between the Q output and the complementary Q output, and the first input of the first NAND gate and the third input of the second NAND gate.

Claims 40 – 41. (Cancelled)

42. (Previously Presented) The SR flip-flop of claim 39 in which the slave JK flip-flop comprises a NAND-gate based flip-flop.

43. (Previously Presented) The SR flip-flop of claim 39 in which the slave JK flip-flop comprises a NOR-gate based flip-flop.

44. (Cancelled).

45. (Previously Presented) The SR flip-flop of claim 39 further comprising at least one controlled power supply coupled to the slave JK flip-flop.

Claims 46 - 48. (Cancelled)

49. (Previously Presented) The SR flip-flop of claim 39 in which the slave JK flip-flop comprises a non-volatile ferroelectric flip-flop.

50. (Previously Presented) The SR flip-flop of claim 39 in which the slave JK flip-flop comprises a ferroelectric capacitor circuit including first, second, and third ferroelectric capacitors.

51. (Previously Presented) The SR flip-flop of claim 50 in which one of the ferroelectric capacitors comprises two serially-coupled matched ferroelectric capacitors.

52. (Previously Presented) The SR flip-flop of claim 50 further comprising means for selectively coupling the ferroelectric capacitor circuit.

53. (Cancelled).

54. (Previously Presented) The SR flip-flop of claim 39 further comprising a precharge circuit coupled to the slave JK flip-flop.

55. (Cancelled).

56. (Previously Presented) The SR flip-flop of claim 39 further comprising an equalization circuit coupled to the slave JK flip-flop.

57. (Cancelled).

58. (Previously Presented) The SR flip-flop of claim 39 further comprising a gate control circuit coupled to the slave JK flip-flop.

59. (Cancelled).

60. (Previously Presented) The SR flip-flop of claim 39 in which the slave JK flip-flop further comprises an internal drive isolation circuit.

Claims 61-80 (Cancelled).

81. (Previously Presented) A ferroelectric, non-volatile, SR flip-flop comprising:

a set input;

a reset input;

a Q output;

a complementary Q output;

a first logic gate having an internal circuit node, a first input coupled to the set input, a second input coupled to the output, and an output coupled to the complementary Q output;

a second logic gate having an internal circuit node, a first input coupled to the reset input, a second input coupled to the complementary Q output, and an output coupled to the Q output; and

a ferroelectric capacitor circuit including at least one ferroelectric load capacitor and at least one ferroelectric storage capacitor coupled between the internal node of the first logic gate and the internal node of the second logic gate.